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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/684,843	10/14/2003	Shahriar Rokhsaz	X-1036-1C US	3524

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EXAMINER
SHINGLETON, MICHAEL B

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 03/31/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No. 10-684,843	Applicant(s) Rokhsaz	
	Examiner SHINGLETON	Group Art Unit 2817	

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE Three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

☐ Responsive to communication(s) filed on ______________________.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-12 ~~is~~/are pending in the application.

Of the above claim(s) ______________________ is/are withdrawn from consideration.

☐ Claim(s) ______________________ is/are allowed.

☒ Claim(s) ~~[illegible]~~ 1-12 ~~is~~/are rejected.

[illegible] ______________________ [illegible]

☐ Claim(s) ______________________ are subject to restriction or election requirement

Application Papers

☐ The proposed drawing correction, filed on __________ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on __________ is/are objected to by the Examiner

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119 (a)-(d).

☐ All ☐ Some* ☐ None of the:

☐ Certified copies of the priority documents have been received.

☐ Certified copies of the priority documents have been received in Application No. __________.

☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a))

*Certified copies not received: ______________________.

Attachment(s)

☒ Information Disclosure Statement(s), PTO-1449, ~~Paper No(s).~~ ✓

☒ Notice of Reference(s) Cited, PTO-892

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Interview Summary, PTO-413

☐ Notice of Informal Patent Application, PTO-152

☐ Other ______________

Office Action Summary

U.S. Patent and Trademark Office
PTO-326 (Rev. 11/00)

Part of Paper No. 3/11/04

*U.S. GPO: 2000-472-999/43204

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2 and 4-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanji 6,201,443 (Tanji) in view of Ho 5,889,432 (Ho).

Figure 2 of Tanji discloses an amplifier arrangement having an amplifier circuit 20 that includes an input voltage V_{INP} and V_{INN} and an output voltage V_{OUTP} and V_{OUTN}. The input voltage is amplified by the gain factor (See column 4, around line 38). Transistors M1 and M2 form part of a "feed-forward" boost circuit which is coupled to the intermediate output node, i.e. the nodes connected to the output. Figure 2 of Tanji clearly illustrates the feed-forward boost circuit as receiving the input voltage. When the control voltage is between the two extremes the gain varies wherein the feed-forward boost circuit increases the gain across the entire frequency response including at "higher frequencies" (See column 3 around line 38). Note that the examiner must give the broadest reasonable interpretation to the claims in light of the specification. Tanji does not show the use of inductors in the power supply side of the amplifier arrangement. However, the use of such is very conventional so as to block AC to and from the power supply voltage. Note unmarked inductors shown in Figure 1 of Ho that are directly connected to the power supply 104. Also note column 2, around line 27 of Ho.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided blocking inductors each directly connected to the Power supply V_{DD} in the two main power supply paths of Tanji so as to block ac to and from the power supply voltage as taught by Ho. Note that just like applicant's disclosed invention the inclusion of these two inductors allows the applicant's to be called an "inductive amplifier" and accordingly the invention made obvious above is an "inductive amplifier".

The invention made obvious above clearly includes the structure of a first half-circuit having a first inductor, a first resistor R_1 and a first transistor M_3 connected in series with a first current supply M_6, wherein a first intermediate output node is located between the first resistor and the first inductor.

The invention made obvious above also clearly includes a second half-circuit having a second inductor, a second resistor R_2 and a second transistor M_4 connected in series with the first current supply M_6, wherein a second intermediate output node is located between the second resistor R_2 and the second inductor, and wherein the first half-circuit is connected in parallel with the second half-circuit.

The invention made obvious above also clearly includes a gate of the first transistor M_3 and a gate of the second transistor M_4 are configured to receive differential input voltage signals, wherein the input voltage comprises a differential input voltage of the differential input signals, and wherein the gate of the first transistor receives the differential input voltage.

The invention made obvious above also clearly includes the feed-forward boost circuit further having a second current source M_5, a first boost transistor M_1 coupled between the first intermediate node and the second current source M_5 wherein a gate of the first boost transistor receives the differential input voltage and a second boost transistor M_2 coupled between the second intermediate output node and the second current source.

The invention made obvious above also clearly includes the elements of the feed-forward boost circuit being selected such that the gain of the inductive amplifier is boosted at frequencies greater than the 3db cut-off frequency of the inductive amplifier circuit. The examiner must give the broadest reasonable interpretation to the claimed invention consistent that the specfication. Clearly the feed-forward boost circuit boosts the gain as compared to when just the main amplifier circuit composed of at least elements $M_3 M_4$ are active. Thus, at the 3bB cut-off frequency inherently is increased when the overall gain is increased by the feed-forward boost circuit.

The invention made obvious above also clearly provides for the method steps of generating at least part of a primary current through transistors M3, M4 in the inductive amplifier in response to a differential input of a pair of differential input signals, generating at least part of a feed-forward current through transistors M1, M2 in response to the differential input signal, and combining the at least part of the primary current with the at least part of the feed-forward current whereby the at least part of the feed-forward current increases at least in part the gain of the inductive amplifier circuit (See column 3, around line 38). Also the step of wherein the at least part of the primary current is generated by applying the differential input signal to a first transistor M_3, whereby the at least part of the primary current flows through the first transistor, a load resistor R_1 and an inductor is clearly provided for in the structure made obvious above. Because at least part of the feed-forward current flows through the load resistor R_1 this provides for the step of applying the at least part of the feed-forward current to an intermediate node between the load resistor and an inductor is clearly provided for in the structure made obvious above.

Also the step of wherein the at least part of the feed-forward current is generated by applying the differential input signal to a second transistor, whereby the at least part of the feed-forward current flows through the second transistor is clearly provided for in the structure made obvious above. The limitation of "wherein the inductive amplifier circuit provides an acceptable gain for differential input signals having frequencies greater than 1 Giga-Hertz" is a broad limitation because of the term "acceptable". Any gain can be considered to be "acceptable".

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanji 6,201,443 (Tanji) in view of Ho 5,889,432 (Ho) as applied to claims 1, 2 and 4-12 above, and further in view of Applicant's Admitted Prior art as represented by Figure 1 (AAPA).

All the reasoning above as applied to claims 1, 2 and 4-12 and the following. Tanji and Ho fails to show or suggest the use of a capacitor or capacitors connected across the first and second intermediate nodes.

AAPA teaches the use of two capacitors connected on the non-power supply sides of the inductors L1 and L2. This clearly provides for improved filtering as well as resonant effects.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided one or more capacitors connected across the first and second intermendiate node of the invention made obvious above so at to improve filtering and provide for resonant effects as taught by AAPA.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wilson 6,552,612 and Cargill 5,903,185 both show similar arrangements to the applied Tanji reference. Asai and Colinge et al. disclose general state of the art circuits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is 571-272-1770. The examiner can normally be reached on Monday-Thursday from 8:00 to 4:30. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (571)-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

MBS
March 11, 2004

MICHAEL B. SHINGLETON
PRIMARY EXAMINER
GROUP ART UNIT 2817